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LOW DISTORTION AND HIGH SLEW RATE OUTPUT STAGE FOR VOLTAGE FEEDBACK AMPLIFIER

TECHNICAL FIELD

[001] The present invention relates to voltage feedback ("VF") operational amplifier ("op amp") circuits, specifically circuits configured as high speed, full bandwidth operational amplifiers.

BACKGROUND OF THE INVENTION

[002] The VF op amp is one of the most common types of op amps. High speed VF op amps are used in a variety of circuits, including arbitrary waveform generators, high linearity analog to digital converters ("ADC"), preamplifiers, digital to analog converters ("DAC"), output buffers, active filters and wireless communication receivers. In a typical VF op amp, there are two inputs, a positive input and a negative input, and one output. Across the two inputs, an error voltage (V_e) is developed. The output voltage (V_o) of the op amp is obtained by multiplying "a" by V_e , where "a" is the open loop voltage gain of the op amp. When negative feedback is applied from the output of the op amp across a resistor divider network, for example R_1 and R_2 , to the negative input, the action of the op amp is to drive V_e to zero. This topology defines the VF op amp. Voltage feedback reduces the gain and stabilizes the VF op amp. In this situation, gain can be set by the ratio of R_1 to R_2 . However, the gain of the VF op amp is

frequency dependent. It is well known that the closed loop gain and closed loop bandwidth remain substantially constant over most of the frequencies of operation. Thus, if gain is increased, bandwidth is reduced and vice versa. As used herein, the term fast refers to the ability of the op amp to accurately reproduce high and extremely high frequency signals.

[003] A conventional class AB op amp circuit 100 is seen in Figure 1. This op amp circuit 100 comprises an input stage 101 with a common base gain stage 102 and a classic diamond driver 103, comprised of transistors Q22 22, Q23 23, Q24 24, and Q25 25. The front end of op amp circuit 100 comprised of input stage 101 and gain stage 102 contribute to a fast op amp configuration. Input stage 101 is fast due to the fact that the current coming out of transistors Q11 11, Q33 33, Q99 99 and Q10 10 change exponentially with the error voltage V_e . If the signal is increased then more error voltage is developed and as a consequence more current is delivered from input stage 101. Gain stage 102 is fast because it is driven by the exponential currents from input stage 101. These exponential currents increase or decrease the base to emitter voltage (V_{BE}) on transistors Q13 13 and Q15 15. This voltage becomes a current that changes exponentially with V_{BE} . Output stage 103 of op amp circuit 100 is a limiting factor in terms of speed of the overall circuit because when the signal being fed therein is too fast, the current from static current sources comprised of transistors Q48 48 and Q50 50 feeding the pre-drivers, comprising transistors Q22 22, and Q23 23, decreases due to parasitic capacitance (C_{BC} and C_{BE}) associated with transistor Q48 48 and transistor Q50 50. Less current reduces the speed of these transistors. In other words, these transistors react slower to a signal when it has less current through them. The parasitic capacitance C_{BC} or C_μ is a capacitance caused by the depletion region in a reverse biased PN junction. The parasitic capacitance C_{BE} or C_π is a capacitance caused by the depletion region in forward biased PN junction. What is desired is a high speed

VF op amp with a high slew rate adapted to provide full power bandwidth and lower distortion at higher frequencies. Full power bandwidth indicates how fast an amplifier is able to perform. It is a different way of measuring slew rate which is a measurement of the speed of the amplifier.

SUMMARY OF THE INVENTION

[004] The present invention achieves technical advantages as an op amp circuit operable to provide a dynamic bias from a common base gain stage to pre-drivers of an output stage. This arrangement allows the op amp to achieve a higher slew rate without any discontinuity in the signal and without an increase in power dissipation. Numerous advantages are provided by the invention, including but not limited to, the ability to achieve full power bandwidth and lower distortion at higher frequencies and/or higher signal amplitudes. These and other advantages related to the invention will become apparent to persons skilled in the relevant arts through careful reading of the disclosure and claims presented herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[005] For a better understanding of the invention including its features, advantages and specific embodiments, reference is made to the following detailed description along with accompanying drawings in which:

[006] Figure 1 illustrates a conventional op amp used to increase full power bandwidth;

[007] Figure 2 is a step response plot at the output of the op amp of Figure 1;

[008] Figure 3 depicts the operational amplifier of the present invention showing the dynamic bias configuration at the output stage;

[009] Figure 4 is a pulse response plot of the operational amplifier of the present invention; and

[010] Figure 5 is a composite plot of the falling edge of the pulse response of the conventional operational amplifier and the operational amplifier of the present invention.

[011] References in the detailed description correspond to like references in the figures unless otherwise noted. Descriptive and directional terms such as top, bottom, left, right, first, second, refer to the drawing itself as laid out on the paper and not to physical limitations of the invention unless specifically noted.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

[012] While a single configuration of the present invention is discussed in detail below, it should be appreciated that the present invention provides many applicable inventive concepts which can be embodied in a wide variety of specific contexts.

[013] Figure 1 illustrates a conventional op amp circuit 100. As seen therein, it includes an input stage 101 with a single gain stage 102 and a unity gain output stage 103. To achieve the highest full power bandwidth, the gain stage 102 is typically based on a common base architecture so that the secondary poles are at very high frequencies.

[014] Output stage 103, is a diamond driver comprised of transistors Q22 22, Q23 23, Q24 24, and Q25 25. The circuit of Figure 1 is inherently fast, however, when the signal being fed therein is too fast, the current from the static current sources comprised of transistors Q48 48 and Q50 50 feeding the pre-drivers comprised of transistors Q22 22 and Q23 23 will decrease the speed of the op amp circuit due to the parasitic capacitance C_{BC} and C_{BE} associated with transistors Q48 48 and Q50 50.

[015] Figure 2 is a plot 201 illustrating the step response at the output of the conventional op amp circuit 100 of Figure 1. From the plot 201 of Figure 2, it can be noted that the pulse has a limited slew rate. It also shows a discontinuity when the signal is transitioning from one level to another. This discontinuity contributes to the decrease in the slew rate. In order to overcome these disadvantages, a circuit arrangement is desired that provides a dynamic bias from the common base gain stage 102 to the pre-drivers of the output stage 103 so that a higher slew rate is achieved without any discontinuity.

[016] Figure 3 depicts an embodiment of an op amp circuit 300 of the present invention. This op amp is configured as a class AB op amp. In contrast to the conventional circuit of Figure

1, op amp circuit 300 of the present invention utilizes a dynamic bias at output stage 303 provided by transistor Q38 338, Q39 339, Q40 340 and Q41 341. Transistors Q38 338 and Q39 339 are driven by current from transistors Q36 336 and Q37 337. As seen therein, the emitters of transistor Q42 342 and transistor Q43 343 are coupled such that they will copy the source current or sink current at high impedance nodes 304 and 305 at the collectors of Q36 336 and Q37 337 from gain stage 302. Further, as seen therein, transistor Q36 336 and transistor Q37 337, are used to create the high impedance nodes at gain stage 302. Transistors Q42 342, Q43 343, Q36 336 and Q37 337 share the same base-emitter connections. These connections ensure that the current from transistors Q36 336 and Q42 342 are the same, and the current from transistors Q37 337 and Q43 343 are the same.

[017] Figure 4 shows a plot 401 of the pulse response of the op amp circuit 300 of Figure 3. As can be seen therein, the op amp circuit 300 of the present invention has higher slew rate than the conventional op amp circuit 100 of Figure 1, as seen in the plot of Figure 2.

[018] Figure 5 is a composite plot 501 of the falling edge of the pulse response for the conventional op amp circuit 100 and the op amp circuit 300 of the present invention. Plot 503 illustrates the improvement in speed of the op amp circuit 300 over the conventional op amp circuit 100 of Figure 1. The improvement in the slew rate also contributes to the better linearity of the present invention over the conventional op amp circuit 100. The lower distortion of the circuit of the present invention is obtainable because the V_{BE} junction of the pre-drivers, comprised of transistors Q38 338 and Q39 339, varies minimally during signal transitions. This results in minimization of the non-linear capacitance and thus less distortion in the output response. The advantages of this biasing scheme include less distortion and higher slew rate without an increase in power consumption.

[019] The embodiment shown and described above is only exemplary. Even though several characteristics and advantages of the present invention have been set forth in the foregoing description together with details of the method of the invention, the disclosure is illustrative only and changes may be made within the principles of the invention to the full extent indicated by the broad general meaning of the terms used in the attached claims. Reference to specific npn and pnp transistors herein or in the Figures is not meant to be limiting as these transistor types can be switched depending on the polarity of the applied signals.